ZDW
AF#

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 09/824,890
Filed: April 2, 2001
Inventor(s):
Kevin J. McGrath, Michael T. Clark, and James B. Keller

Title: Establishing an Operating Mode in a Processor

§ § § § § § § § § § § § § § § §

Examiner: Li, Aimee J.
Group/Art Unit: 2183
Atty. Dkt. No: 5500-54701

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

Lawrence J. Merkel
Printed Name

Signature

3/11/05
Date

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir/Madam:

Further to the Notice of Appeal filed January 21, 2005, Appellants present this Appeal Brief. Appellants respectfully request that this appeal be considered by the Board of Patent Appeals and Interferences.

I. REAL PARTY IN INTEREST

The present application is owned by Advanced Micro Devices, Inc., a corporation organized and existing under and by virtue of the laws of the State of Delaware, and having its principal place of business at One AMD Place, Sunnyvale, CA 94088, as evidenced by the assignment recorded at Reel 011766, Frame 0581.

II. RELATED APPEALS AND INTERFERENCES

This appeal is related to an appeal filed in the parent case of the present application. The parent case is Application Serial No. 09/483,101, filed on January 14, 2000. The appeal number is 2004-1122. No decision has been received by the Appellants in the related appeal as of the date that this appeal brief is filed.

III. STATUS OF CLAIMS

Claims 1-51 are pending. Claims 1-6, 14-24, 26-36, and 49-51 are rejected, and the rejection of these claims is being appealed. Appellants note that the summary sheet of the Final Office Action mailed October 21, 2004 ("Final Office Action") states that claims 1-36 and 49-51 are rejection. However, the Final Office Action contains no rejection of claims 7-13 and 25. Accordingly, Appellants are presuming for this appeal that claims 7-13 and 25 are objected to but would be allowable in independent form, similar to claims 37-48. A copy of claims 1-51 is included in the Claims Appendix attached hereto.

IV. STATUS OF AMENDMENTS

No amendments to the claims have been submitted subsequent to the final rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 is directed to an apparatus comprising a first storage location (Figs. 1 or 13, reference numeral 24A; Figs. 19, 20, or 21, reference numeral 1054), a second storage location (Figs. 1 or 13, reference numeral 26; Figs. 19, 20, or 21, reference numeral 1056), and a processor (Figs. 1 or 13, reference numeral 10; Figs. 19, 20, or 21, reference numeral 1042). The first storage location is configured to store a segment selector (Fig. 1, reference numeral 24AA) identifying a segment descriptor (Fig. 1, reference numeral 24AB and Figs. 2 and 3) including a first operating mode indication (Figs. 2 and 3, reference numeral 42), a second operating mode indication (Figs. 2 and 3, reference numeral 44), and one or more indications that identify a segment described by the segment descriptor as a code segment (Figs. 2 and 3, reference numeral 52). The second storage location is configured to store an enable indication (LMA or LME), wherein the enable indication, the first operating mode indication, and the second operating mode indication are indicative of a default address size (Figs. 5 and 6). The processor is configured to process an instruction using the default address size. See, e.g., specification, page 6, lines 17-27; page 7, lines 17-24; page 8, line 22-page 9, line 3; page 13, lines 20-23; page 19, line 6-page 20, line 24; page 35, line 3-page 36, line 10; page 44, lines 5-14; and page 47, lines 11-18.

Independent claim 23 is directed to a method comprising determining a default address size in response to an enable indication in a first storage location (Figs. 1 or 13, reference numeral 26; Figs. 19, 20, or 21, reference numeral 1056), a first operating mode indication (Figs. 2 and 3, reference numeral 42) in a segment descriptor (Figs. 2 and 3), and a second operating mode indication (Figs. 2 and 3, reference numeral 44) in the segment descriptor; and generating addresses in response to the default address size. The segment descriptor further includes one or more indications that identify a segment described by said segment descriptor as a code segment (Figs. 2 and 3, reference numeral 52). See, e.g., specification, page 6, lines 17-27; page 7, lines 17-24; page 8, line 22-page 9, line 3; page 13, lines 20-23; page 19, line 6-page 20, line 24; page 35, line 3-page 36, line 10; page 44, lines 5-14; and page 47, lines 11-18.

Independent claim 34 is directed to a computer readable medium (Fig. 22, reference numeral 1090) storing a plurality of native instructions (Fig. 22, reference numeral 1092 or 1094) executable directly on a processor, wherein the plurality of native instructions comprise native instructions which, when executed, perform one or more operations defined for a non-native instruction using a default address size, the default address size determined in response to an enable indication in a first storage location (Figs. 1 or 13, reference numeral 26; Figs. 19, 20, or 21, reference numeral 1056), a first operating mode indication (Figs. 2 and 3, reference numeral 42) in a segment descriptor (Figs. 2 and 3), and a second operating mode indication (Figs. 2 and 3, reference numeral 44) in the segment descriptor. The segment descriptor further includes one or more indications that identify a segment described by said segment descriptor as a code segment (Figs. 2 and 3, reference numeral 52). See the above specification citations as well as page 47, line 20-page 48, line 10.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1, 14-20, 23, 34-35, and 49-51 stand rejected under 35 U.S.C. § 102(b) as being anticipated by James L. Turley's Advanced 80386 Programming Techniques ("Turley").

2. Claims 26-31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Turley in view of Schrofer, U.S. Patent No. 4,682,284 ("Schrofer").

3. Claim 21 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Turley in view of Park, U.S. Patent No. 6,021,484 ("Park").

4. Claim 36 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Turley in view of Hennessy and Patterson's Computer Architecture, a Quantitative Approach ("Hennessy").

5. Claims 23-24 and 32-33 stand provisionally rejected under 35 U.S.C. § 101 over claims 17-18 and 21-33 of U.S. Patent Application Serial No. 09/483,101.

6. Claims 1-6 and 22 stand provisionally rejected under the judicially-created doctrine of obviousness-type double patenting over claims 1-6 and 10 of U.S. Patent Application Serial No. 09/483,101.

VII. ARGUMENT

First Ground of Rejection:

Claims 1, 14-20, 23, 34-35, and 49-51 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Turley. Appellants traverse this rejection for the following reasons.

Claims 1, 14, 16-17, and 19:

Appellants respectfully submit that claim 1 recites a combination of features not taught or suggested in Turley. For example, claim 1 recites a combination of features including: "a first storage location configured to store a segment selector identifying a segment descriptor including a first operating mode indication, a second operating mode indication, and one or more indications that identify a segment described by said segment descriptor as a code segment; [and] a second storage location configured to store an enable indication, wherein said enable indication, said first operating mode indication, and said second operating mode indication are indicative of a default address size". Turley does not teach or suggest the above highlighted features.

The Final Office Action, in the Response to Remarks section, alleges that the first operating mode indication is anticipated by Turley's privilege level (DPL) and that the second operating mode indication is anticipated by Turley's granularity bit (G). (See Final Office Action, pages 12-13, table entries for first operating mode indication (bottom of page 12) and second operating mode indication (top of page 13)). Appellants respectfully disagree.

With regard to the privilege level (DPL), Appellants respectfully submit that Turley has no teaching or suggestion that the DPL is in any way related to default address size. Turley teaches: "This 2-bit field indicates the level of privilege associated with the memory space that the descriptor defines. DPL 0 is most privileged, and DPL 3 the least" (Turley, page 51, paragraph 5). Additionally, Turley teaches the following with regard to privilege level: "Working closely with memory management is a relatively new system of privileged checking...with this method, every piece of code and data is assigned one of four privilege levels, and the processor automatically performs privilege validation on every memory cycle. If the application is privileged enough, its memory access will be granted. If not, the processor will deny access and generate a privilege fault; the operating system will then take over." (Turley, page 10, last paragraph continuing on to page 11). Thus, the privilege level may be used in determining if a memory access is granted or denied. Granting or denying the memory access is independent of the address size and does not affect the address size in any way. Appellants respectfully submit that there is no teaching or suggestion in Turley that the privilege level is a first operating mode indication, wherein "said enable indication, *said first operating mode indication*, and said second operating mode indication are *indicative of a default address size*". Appellants respectfully submit that, since the DPL does not teach the first operating mode indication, the rejection fails for at least this reason.

The Final Office Action further alleges that "the DPL bit must match to allow access to the segment of memory. If access is not granted to the segment of memory, the segment cannot be accessed to set the address size" (Final Office Action, page 14, lines 15-17 in the right-hand box). **Appellants respectfully submit that there is nothing in the Turley's segment that sets the address size, or any other attribute of the segment**. The segment is merely the memory region that is described by the segment descriptor, and may store instructions or data (See, e.g., Turley page 48, "Segment Descriptors" section). **Segment attributes, *including default address size*, are determined from Turley's segment descriptor, and the DPL field does not control access to the segment descriptor**. The DPL field is IN the segment descriptor, and thus the segment descriptor must be accessed to even determine the value of the DPL field

(See Turley, page 50, Figure 2-2). Also, Turley defines the DPL as "This two bit field indicates the level of privilege associated with the *memory space that the descriptor defines*" i.e., the segment (Turley, page 51, fifth paragraph). Accordingly, it is clear that the DPL field does not control access to the segment descriptor, and that the segment descriptor determines the attributes of the segment (and thus there is no access to the segment itself to determine address size). Turley teaches that "A program that tries to traverse the entire 4GB address space of the 80386 merely by incrementing an index repeatedly would probably be greeted by a segment violation exception at some point along the way" (Turley, page 47, lines 3-6). Thus, Turley teaches that addresses are generated, and the generated address causes a segment violation exception. Thus, while the access is not permitted, the size of the address is not limited by the occurrence of the exception.

The Final Office Action concludes that "in order to establish a default address size...the DPL must indicate that segment memory is accessible" (Final Office Action, page 14, lines 22-25 in the right-hand box). As highlighted above, there is simply no support for this assertion in Turley. While the DPL may determine if the segment is accessible, it has no effect on the default address size since the default address size is determined from the segment descriptor, not the segment itself.

Furthermore, Turley teaches the following regarding the granularity (G) bit: "When this bit is cleared, the 20-bit limit field is assumed to be measured in units of 1 byte. If it is set, the limit field is in units of 4096 bytes" (Turley, page 52, third paragraph). Turley further teaches: "The granularity bit allows you to build a segment larger than 1 MB." (Turley, page 54, second paragraph). Thus, the granularity bit, in conjunction with the limit field, defines the size of a segment. This does not teach or suggest a second operating mode indication wherein "said enable indication, said first operating mode indication, and *said second operating mode indication* are *indicative of a default address size*". The G bit determines how to interpret the limit field, and defines the size of the segment. Addresses of the default address size (which is NOT determined by the G bit) would be used to address the segment, independent of the value of the G bit.

While an address of the default address size may exceed the limit (and thus result in a segment violation exception, as highlighted above), the G bit and the segment limit have no effect on the default address size itself.

The rejection of claim 1 in the Final Office Action also refers to various portions of Turley more generally with respect to the first and second operating mode indications. More particularly, the Final Office Action alleges that Turley teaches the first and second operating mode indications at page 49, table: A segment descriptor; pages 47-48, paragraphs 5 to 2; page 50, Figure 2-2; page 51-52; page 53, paragraph 3; and page 54, Table (See Final Office Action, page 4, item 15a). With such general recitations of teachings, it is unclear exactly what in Turley's segment descriptor is alleged to be the first and second operating mode indications. However, the table labeled "A segment descriptor" on page 49 merely generally describes a segment descriptor, and offers no details. Pages 47-48 have a general description of segment descriptors, but nothing in this section teaches or suggests the above highlighted features of claim 1. Pages 50-54 describe a segment descriptor in more detail, and describe the various bits. Nothing in the description of Turley's segment descriptor indicates that Turley's segment descriptor includes a first operating mode indication and a second operating mode indication as recited in claim 1. The Final Office Action also refers to page 178, paragraphs 2 and 3 of Turley. This section of Turley describes the use of task state segments (TSS), and appears to have nothing to do with the above highlighted features of claim 1.

The Final Office Action, in the Response to Remarks section, alleges that the claims do not exactly specify what "address size" refers to, because address size could refer to the size of the address space or the number of bits needed to represent a valid address. Appellants respectfully submit that the term "address size" is well understood in the art to refer to the number of bits in an address.

Accordingly, Appellants respectfully submit that claim 1 is patentable over Turley for at least the above stated reasons. For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 1 over Turley is in error and

request reversal of the rejection. Claims 14, 16-17, and 19 depend from claim 1 and thus are patentable over Turley for at least the above stated reasons as well. Each of claims 14, 16-17, and 19 recite addition combinations of features not taught or suggested in Turley.

Claims 15 and 18

Claim 15 depends from claim 1, and thus is patentable over Turley for the reasons given above for claim 1. Additionally, claim 15 recites a combination of features including: "said first storage location [configured to store a segment selector identifying a segment descriptor including a first operating mode indication, a second operating mode indication, and one or more indications that identify a segment described by said segment descriptor as a code segment, from claim 1] is a general purpose register within said processor". Appellants respectfully disagree.

To support this rejection, the Final Office Action cites Turley's teachings of a segment register, which is a special purpose register. The Final Office Action then states "a general purpose register, by definition, is a register that can be used for different purposes, including as a special handler of data, which means that a register which handles special data, such as a segment register, is a type of general purpose register...see Rosenberg's Dictionary of Computers, Information Processing, and Telecommunications 2nd Edition" (Final Office Action, page 6, lines 12-17). Appellants respectfully disagree that a special purpose register is a type of general purpose register, as one of skill in the art would interpret those terms.

Furthermore, Rosenberg's definitions contradict the Final Office Action's assertion. Rosenberg defines a general purpose register as "a register...that can be used for different purposes, for example as an accumulator, as an index register, or as a special handler of data" (Rosenberg, page 256). Rosenberg defines special purpose register as "a CPU register **dedicated** to a specific function and **available for that purpose only**". These definitions contradict any assertion that a special purpose register is a type of general purpose register, as a special purpose register cannot be used for different

purposes. Accordingly, Turley's special purpose segment register does not teach or suggest "said first storage location is a general purpose register within said processor" as recited in claim 15.

Claim 18 depends from claim 1, and thus is patentable over Turley for the reasons given above for claim 1. Additionally, claim 18 recites a combination of features including: "said second storage location [configured to store an enable indication, from claim 1] is a general purpose register within said processor". Appellants respectfully disagree, for reasons similar to those given above. Turley teaches a special purpose control register (CR0), which is not a general purpose register.

Accordingly, Appellants respectfully submit that claims 15 and 18 are patentable over Turley for at least the above stated reasons. For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claims 15 and 18 over Turley is in error and request reversal of the rejection.

Claim 20

Claim 20 depends from claim 1, and thus is patentable over Turley for the reasons given above for claim 1. Additionally, claim 20 recites a combination of features including: "said processor is configured to process said instruction by executing interpreter software which emulates said instruction".

The Final Office Action alleges that Turley teaches the above highlighted features in pages 283-286. However, pages 283-286 are the beginning of a chapter in Turley on 8086 Emulation. 8086 emulation is provided via a compatibility mode, referred to as virtual 8086 mode, or VM86 (see Turley, page 284, third paragraph). In this mode, the 80386 runs older code unmodified (Turley, page 284, fourth paragraph). You enter VM86 mode by setting a VM flag in the EFLAGS register (Turley, page 286, first paragraph). Thus, the 8086 emulation is provided in the 80386 as a processor mode in which the processor directly executes the 8086 instructions using 8086-style execution. If the VM86 mode is not active, 80386 instructions are directly executed. That is, the

processor is always directly executing the instructions in the programs that have been launched by the user.

None of these teachings regarding VM86 mode teaches or suggests "said processor is configured to process said instruction by executing *interpreter software* which emulates said instruction" as recited in claim 20. Accordingly, Appellants respectfully submit that claim 20 is patentable over Turley for at least the above stated reasons. For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claims 20 over Turley is in error and request reversal of the rejection.

Claim 23

Appellants respectfully submit that claim 23 recites a combination of features not taught or suggested in Turley. For example, claim 23 recites a combination of features including: "determining a default address size in response to an enable indication in a first storage location, a first operating mode indication in a segment descriptor, and a second operating mode indication in said segment descriptor, wherein said segment descriptor further includes one or more indications that identify a segment described by said segment descriptor as a code segment".

The Final Office Action relies on the same teachings from Turley to allegedly teach the first and second operating modes in claim 23 as were relied on for claim 1 (namely, the DPL, the G bit, page 49, table: A segment descriptor; pages 47-48, paragraphs 5 to 2; page 50, Figure 2-2; page 51-52; page 53, paragraph 3; and page 54, Table). These teachings, highlighted above with regard to claim 1, also do not teach or suggest the first operating mode indication and the second operating mode indication recited in claim 23.

Additionally, the Final Office Action cites Turley's page 176, paragraph 1 and page 178, paragraphs 2-3 with regard to "in response to an enable indication in a first storage location" as recited in claim 23. However, page 176, paragraph 1 and page 178, paragraphs 2-3 describe the task state segment (TSS) and how it can be used for task

switching. This has nothing to do with the above highlighted features, nor "determining a default address size in response to an enable indication in a first storage location..." as recited in claim 23.

Accordingly, Appellants respectfully submit that claim 23 is patentable over Turley for at least the above stated reasons. For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 23 over Turley is in error and request reversal of the rejection.

Claims 34, 49, and 51

Appellants respectfully submit that claim 34 recites a combination of features not taught or suggested in Turley. For example, claim 34 recites a combination of features including: "the default address size determined in response to an enable indication in a first storage location, a first operating mode indication in a segment descriptor, and a second operating mode indication in said segment descriptor, wherein said segment descriptor further includes one or more indications that identify a segment described by said segment descriptor as a code segment". The same teachings of Turley highlighted above with regard to claim 1 are alleged to teach the above highlighted features of claim 34. For reasons similar to those highlighted above with regard to claim 1, Turley does not teach or suggest the above highlighted features of claim 34. For example, Turley's DPL and G bit do not teach or suggest the first operating mode indication and second operating mode indication to determine a default address size.

Furthermore, claim 34 recites a combination of features including: "A computer readable medium storing a plurality of native instructions executable directly on a processor, wherein the plurality of native instructions comprise native instructions which, when executed, perform one or more operations defined for a non-native instruction". The Final Office Action alleges that Turley teaches the above features in pages 283-286. Appellants respectfully disagree.

Pages 283-286 are the beginning of a chapter in Turley on 8086 Emulation.

However, 8086 emulation is provided via a compatibility mode, referred to as virtual 8086 mode, or VM86 (see Turley, page 284, third paragraph). In this mode, the 80386 runs older code unmodified (Turley, page 284, fourth paragraph). You enter VM86 mode by setting a VM flag in the EFLAGS register (Turley, page 286, first paragraph). Thus, the 8086 emulation is provided in the 80386 as a processor mode in which the processor directly executes the 8086 instructions using 8086-style execution. If the VM86 mode is not active, 80386 instructions are directly executed.

None of the above teaches or suggest "a plurality of native instructions executable directly on a processor, wherein the plurality of native instructions comprise *native instructions* which, when executed, perform *one or more operations defined for a* ***non-native*** *instruction*".

Accordingly, Appellants respectfully submit that claim 34 is patentable over Turley for at least the above stated reasons. For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 34 over Turley is in error and request reversal of the rejection. Claims 49 and 51 depend from claim 34 and thus are patentable over Turley for at least the above stated reasons as well. Each of claims 49 and 51 recite addition combinations of features not taught or suggested in Turley.

Claim 35

Claim 35 depends from claim 34, and thus is patentable over Turley for the reasons given above for claim 34. Additionally, claim 35 recites a combination of features including: "the native instructions emulate the non-native instruction".

With respect to claim 35, the Final Office Action again cites Turley's 8086 emulation chapter, pages 283-286. However, as noted above, Turley's 8086 emulation refers to a mode in the 80386 processor in which the processor directly executes 8086 instructions. Thus, these teachings also do not teach or suggest "the native instructions emulate the non-native instruction" as recited in claim 35.

Accordingly, Appellants respectfully submit that claim 35 is patentable over Turley for at least the above stated reasons. For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 35 over Turley is in error and request reversal of the rejection.

Claim 50

Claim 50 depends from claim 34, and thus is patentable over Turley for the reasons given above for claim 34. Additionally, claim 50 recites a combination of features including: "said first storage location [that stores an enable indication, from claim 34] is a general purpose register within said processor".

To support this rejection, the Final Office Action cites Turley's teachings of the CR0 register, which is a special purpose register. The Final Office Action then states "a general purpose register, by definition, is a register that can be used for different purposes, including as a special handler of data, which means that a register which handles special data, such as a segment register, is a type of general purpose register...see Rosenberg's Dictionary of Computers, Information Processing, and Telecommunications 2nd Edition" (Final Office Action, page 6, lines 12-17). Appellants respectfully disagree that a special purpose register is a type of general purpose register, as one of skill in the art would interpret those terms.

Furthermore, Rosenberg's definitions contradict the Final Office Action's assertion. Rosenberg defines a general purpose register as "a register...that can be used for different purposes, for example as an accumulator, as an index register, or as a special handler of data" (Rosenberg, page 256). Rosenberg defines special purpose register as "a CPU register **dedicated** to a specific function and **available for that purpose only**". These definitions contradict any assertion that a special purpose register is a type of general purpose register, as a special purpose register cannot be used for different purposes. Accordingly, Turley's special purpose CR0 register does not teach or suggest "said first storage location is a general purpose register within said processor" as recited in claim 50.

Accordingly, Appellants respectfully submit that claim 50 is patentable over Turley for at least the above stated reasons. For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 50 over Turley is in error and request reversal of the rejection.

Second Ground of Rejection:

Claims 26-31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Turley in view of Schrofer. Appellants traverse this rejection for the following reasons.

Claims 26-31:

Claims 26-31 depend from claim 23, and thus are patentable over Turley (and Turley in view of Schrofer) for at least the reasons given above for claim 23. Additionally, each of claims 26-31 recites a combination of features not taught or suggested in Turley in view of Schrofer. For example, claim 26 recites a combination of features including: "said second segment descriptor occupies up to two entries of said plurality of entries depending upon a type of said second segment descriptor".

Appellants respectfully submit that the alleged combination of Turley in view of Schrofer does not form a *prima facie* case of obviousness of claim 23 because the combination fails to teach or suggest each and every of claim 23. The Final Office Action relies on Schrofer to teach the concept that multiple storage locations can be used for larger data words, citing Schrofer, col. 8, lines 27-42. Schrofer teaches: "Because a memory request transaction may occupy a plurality of bus cycles--up to three in this illustrative example, as has been described above--a single queue entry, representing a single memory request, occupies up the three storage locations 310." (Schrofer, col. 8, lines 30-34). Thus, Schrofer teaches representing a queue entry using multiple storage locations for multiple transfer cycles on a bus.

The combination of Schrofer and Turley, however, does not teach or suggest "said second segment descriptor occupies up to two entries of said plurality of entries [in said

segment descriptor table] depending upon a type of said second segment descriptor". Turley teaches a variety of segment descriptors (e.g. pages 478-480), all of which are the same size (particularly, 64 bits). Schrofer does not teach segment descriptors having different sizes, either. Thus, even though Schrofer teaches a queue entry that occupies multiple storage locations, this teaching would not lead one of skill in the art to "said second segment descriptor occupies up to two entries of said plurality of entries depending upon a type of said second segment descriptor" because the segment descriptors in the alleged combination are still all the same size and fit in a single segment descriptor table entry. Nothing in either Schrofer or Turley suggests that segment descriptors have any size other than 64 bits, which is one segment descriptor table entry in Turley's segment descriptor table (see, e.g., Turley page 61, bottom paragraph, second to last sentence).

Accordingly, Appellants respectfully submit that claim 26 is patentable over Turley in view of Schrofer for at least the above stated reasons. Claims 27-31 depend from claim 26, and thus are patentable over Turley in view of Schrofer for at least the above stated reasons as well. Each of claims 27-31 recites additional combinations of features not taught or suggested in Turley in view of Schrofer. For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claims 26-31 over Turley in view of Schrofer is in error and request reversal of the rejection.

Third Ground of Rejection:

Claim 21 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Turley in view of Park. Appellants traverse this rejection for the following reasons.

Claim 21:

Claim 21 depends from claim 1, and thus is patentable over Turley (and Turley in view of Park) for at least the reasons given above for claim 1. Additionally, claim 21 recites a combination of features including: "said processor is configured to process said instruction by executing translation software to translate said instruction into one or more native instructions to be executed by said processor".

The Final Office Action alleges that the above features would be obvious in view of Park's teachings of hardware that translates instructions (Park, col. 1, line 57-col. 2, line 8 and col. 2, lines 48-59), alleging that implementing the translation is software is "functionally-equivalent" to implementing the translation in hardware (See Final Office Action, page 10, lines 7-9). Appellants respectfully disagree. Park teaches implementing the translation in hardware separate from the processor, which permits the processor to execute one group of instructions while another group is being translated. See Park, Abstract, lines 6-13. Thus, at least in the case of Park's teachings, implementing the translation in hardware that permits simultaneous translation and execution does not teach or suggest "said processor is configured to process said instruction by executing translation software to translate said instruction into one or more native instructions to be executed *by said processor*".

Accordingly, Appellants respectfully submit that claim 21 is patentable over Turley in view of Park for at least the above stated reasons. For at least all of the above stated reasons, Appellants respectfully submit that the rejection of claim 21 over Turley in view of Park is in error and request reversal of the rejection.

Fourth Ground of Rejection:

Claim 36 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Turley in view of Hennessy. Appellants traverse this rejection for the following reasons.

Claim 36:

Claim 36 depends from claim 34, and thus is patentable over Turley for at least the reasons given above for claim 34. Furthermore, Hennessy does not teach or suggest the features highlighted above with regard to claim 34 either. Thus, the combination of Turley and Hennessy does not teach or suggest the combination of features recited in claim 34. Accordingly, the combination of Turley and Hennessy does not teach or suggest the combination of features recited in claim 36, which includes the combination of features recited in claim 34 and additional features. For at least all of the above stated

reasons, Appellants respectfully submit that the rejection of claim 36 over Turley in view of Hennessy is in error and request reversal of the rejection.

Fifth Ground of Rejection:

Claims 23-24 and 32-33 stand provisionally rejected under 35 U.S.C. § 101. Appellants traverse this rejection for the following reasons.

Claims 23-24 and 32-33:

For a statutory double patenting rejection, the same invention must be claimed twice, where "same invention" refers to identical subject matter (see, e.g., MPEP 804(II)(A)). Appellants respectfully submit that claims 23-24 and 32-33 are not claiming identical subject matter to claims 17-18 and 21-22 of application number 09/483,101. For example, claim 17 of application number 09/483,101 recites:

> establishing a default address size in a processor in response to an enable indication in a control register within said processor, a first operating mode indication in a segment descriptor, and a second operating mode indication in said segment descriptor, said segment descriptor further including one or more bits identifying a segment described by said segment descriptor as a code segment

Claim 23 of the present application recites:

> determining a default address size in response to an enable indication in a first storage location, a first operating mode indication in a segment descriptor, and a second operating mode indication in said segment descriptor, wherein said segment descriptor further includes one or more indications that identify a segment described by said segment descriptor as a code segment

"A control register in said processor" and "a first storage location" are different phrases, and furthermore these phrases differ in scope. Accordingly, a statutory double patenting

rejection is not supported for claim 23 of the present application over claim 17 of application number 09/483,101. Similarly, the statutory double patenting rejection of claim 24 and 32-33 of the present application, which depend from claim 23, over claims 18 and 21-22 of application number 09/483,101, which depend from claim 17, is not supported.

For at least the above reasons, Appellants respectfully submit that the rejection of claims 23-24 and 32-33 under 35 U.S.C. § 101 is in error and request reversal of the rejection.

Sixth Ground of Rejection:

Claims 1-6 and 22 stand provisionally rejected under the judicially-created doctrine of obviousness-type double-patenting. Appellants traverse this rejection for the following reasons.

Claims 1-6 and 22:

In the obviousness-type double-patenting rejection, the Final Office Action states that the claims of application number 09/483,101 contain every element of claims 1-6 and 22 of the instant application and thus anticipates claims 1-6 and 22. Appellants respectfully disagree. For example, claim 1 of application number 09/483,101 recites "a segment register" and "a control register". Claim 1 of the present application recites "a first storage location" and "a second storage location". These are not the same elements. Accordingly, claim 1 of application number 09/483,101 does not anticipate these elements of claim 1 of the present application, as alleged in the rejection.

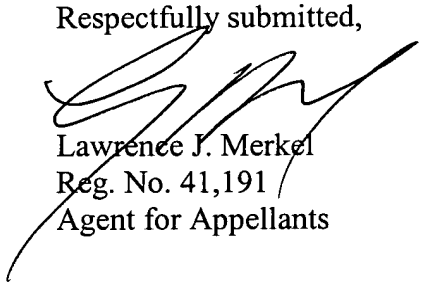
For at least the above reasons, Appellants respectfully submit that the rejection of claims 1-6 and 22 under the judicially-created doctrine of obviousness-type double patenting is in error and request reversal of the rejection.

VIII. CONCLUSION

For the foregoing reasons, it is submitted that the Examiner's rejection of claims 1-6, 14-24, 26-36, and 49-51 was erroneous, and reversal of the decision is respectfully requested.

The Commissioner is authorized to charge the appeal brief fee of $500.00 and any other fees that may be due to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-54701/LJM. This Appeal Brief is submitted with a return receipt postcard.

Respectfully submitted,



Lawrence J. Merkel
Reg. No. 41,191
Agent for Appellants

Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C.
P.O. Box 398
Austin, TX 78767-0398
(512) 853-8850

Date: March 11, 2005

IX. CLAIMS APPENDIX

The claims on appeal are as follows.

1. An apparatus comprising:

a first storage location configured to store a segment selector identifying a segment descriptor including a first operating mode indication, a second operating mode indication, and one or more indications that identify a segment described by said segment descriptor as a code segment;

a second storage location configured to store an enable indication, wherein said enable indication, said first operating mode indication, and said second operating mode indication are indicative of a default address size; and

a processor configured to process an instruction using said default address size.

2. The apparatus as recited in claim 1 wherein said default address size is a first address size if said enable indication is in an enabled state and said first operating mode indication is in a first state, and wherein said default address size is a second address size if said enable indication is in said enabled state, said first operating mode indication is in a second state, and said second operating mode indication is in said first state.

3. The apparatus as recited in claim 2 wherein said second address size is one of a plurality of address sizes available if said enable indication is in said enabled state and said first operating mode indication is in said second state, and wherein said one of said plurality of address sizes is selected in response to a state of said second operating mode indication.

4. The apparatus as recited in claim 3 wherein one of said plurality of address sizes is a 32 bit address size.

5. The apparatus as recited in claim 3 wherein one of said plurality of address sizes is a 16 bit address size.

6. The apparatus as recited in claim 2 wherein said first address size is greater than 32 bits.

7. The apparatus as recited in claim 6 wherein, if said enable indication is in said enabled state and said first operating mode indication is in said first state, said processor is configured to process said instruction using a default operand size of 32 bits.

8. The apparatus as recited in claim 2 wherein said segment descriptor is one of a plurality of segment descriptors stored in a descriptor table including a plurality of entries, and wherein at least one of said plurality of segment descriptors occupies two of said plurality of entries.

9. The apparatus as recited in claim 8 wherein said one of said plurality of segment descriptors is a call gate descriptor.

10. The apparatus as recited in claim 8 wherein said one of said plurality of segment descriptors is an interrupt gate descriptor.

11. The apparatus as recited in claim 8 wherein said one of said plurality of segment descriptors is a trap gate descriptor.

12. The apparatus as recited in claim 8 wherein said one of said plurality of segment descriptors is a task state segment descriptor.

13. The apparatus as recited in claim 8 wherein said one of said plurality of segment descriptors is a local descriptor table descriptor.

14. The apparatus as recited in claim 1 wherein said first storage location is a memory location.

15. The apparatus as recited in claim 1 wherein said first storage location is a general purpose register within said processor.

16. The apparatus as recited in claim 1 wherein said first storage location is a special purpose register within said processor.

17. The apparatus as recited in claim 1 wherein said second storage location is a memory location.

18. The apparatus as recited in claim 1 wherein said second storage location is a general purpose register within said processor.

19. The apparatus as recited in claim 1 wherein said second storage location is a special purpose register within said processor.

20. The apparatus as recited in claim 1 wherein said processor is configured to process said instruction by executing interpreter software which emulates said instruction.

21. The apparatus as recited in claim 1 wherein said processor is configured to process said instruction by executing translation software to translate said instruction into one or more native instructions to be executed by said processor.

22. The apparatus as recited in claim 1 wherein, if said enable indication is in a disabled state, said first operating mode indication is undefined and said second operating mode indication is indicative of said default address size.

23. A method comprising:

determining a default address size in response to an enable indication in a first storage location, a first operating mode indication in a segment descriptor, and a second operating mode indication in said segment descriptor, wherein said segment descriptor further includes one or more indications that identify a segment described by said segment descriptor as a code segment;

generating addresses in response to said default address size.

24. The method as recited in claim 23 wherein said determining comprises selecting a first address size as said default address size responsive to said enable indication being in an enabled state and said first operating mode indication being in a first state, and wherein said first address size is greater than 32 bits.

25. The method as recited in claim 24 further comprising determining a default operand size of 32 bits in response to said enable indication in said first storage location, said first operating mode indication in said segment descriptor, and said second operating mode indication in said segment descriptor.

26. The method as recited in claim 23 wherein said segment descriptor is one of a plurality of segment descriptors stored in a descriptor table having a plurality of entries, the method further comprising reading a second segment descriptor of said plurality of segment descriptors from said segment descriptor table, wherein said second segment descriptor occupies up to two entries of said plurality of entries depending upon a type of said second segment descriptor.

27. The method as recited in claim 26 wherein said second segment descriptor is a call gate descriptor.

28. The method as recited in claim 26 wherein said second segment descriptor is an interrupt gate descriptor.

29. The method as recited in claim 26 wherein said second segment descriptor is a trap gate descriptor.

30. The method as recited in claim 26 wherein said second segment descriptor is a task state segment descriptor.

31. The method as recited in claim 26 wherein said second segment descriptor is a local descriptor table descriptor.

32. The method as recited in claim 24 wherein said determining further comprises selecting a second address size as said default address size responsive to said enable indication being in an enabled state, said first operating mode indication being in a second state, and said second operating mode indication being in said first state, and wherein said second address size is 32 bits.

33. The method as recited in claim 24 wherein said determining further comprises selecting one of a plurality of address sizes as said default address size if said enable indication is in said enabled state and said first operating mode indication is in a second state, and wherein said one of said plurality of address sizes is selected in response to a state of said second operating mode indication.

34. A computer readable medium storing a plurality of native instructions executable directly on a processor, wherein the plurality of native instructions comprise native instructions which, when executed, perform one or more operations defined for a non-native instruction using a default address size, the default address size determined in response to an enable indication in a first storage location, a first operating mode indication in a segment descriptor, and a second operating mode indication in said segment descriptor, wherein said segment descriptor further includes one or more indications that identify a segment described by said segment descriptor as a code segment.

35. The computer readable medium as recited in claim 34 wherein the native instructions emulate the non-native instruction.

36. The computer readable medium as recited in claim 34 wherein the native instructions are generated by compiling the non-native instruction.

37. The computer readable medium as recited in claim 34 wherein said default address size is a first address size if said enable indication is in an enabled state and said first operating mode indication is in a first state, and wherein said default address size is a second address size if said enable indication is in said enabled state, said first operating mode indication is in a second state, and said second operating mode indication is in said first state.

38. The computer readable medium as recited in claim 37 wherein said second address size is one of a plurality of address sizes available if said enable indication is in said enabled state and said first operating mode indication is in said second state, and wherein said one of said plurality of address sizes is selected in response to a state of said second operating mode indication.

39. The computer readable medium as recited in claim 38 wherein one of said plurality of address sizes is a 32 bit address size.

40. The computer readable medium as recited in claim 38 wherein one of said plurality of address sizes is a 16 bit address size.

41. The computer readable medium as recited in claim 37 wherein said first address size is greater than 32 bits.

42. The computer readable medium as recited in claim 41 wherein, if said enable indication is in said enabled state and said first operating mode indication is in said first

state, said native instructions use a default operand size of 32 bits.

43. The computer readable medium as recited in claim 37 wherein said segment descriptor is one of a plurality of segment descriptors stored in a descriptor table including a plurality of entries, and wherein at least one of said plurality of segment descriptors occupies two of said plurality of entries.

44. The computer readable medium as recited in claim 43 wherein said one of said plurality of segment descriptors is a call gate descriptor.

45. The computer readable medium as recited in claim 43 wherein said one of said plurality of segment descriptors is an interrupt gate descriptor.

46. The computer readable medium as recited in claim 43 wherein said one of said plurality of segment descriptors is a trap gate descriptor.

47. The computer readable medium as recited in claim 43 wherein said one of said plurality of segment descriptors is a task state segment descriptor.

48. The computer readable medium as recited in claim 43 wherein said one of said plurality of segment descriptors is a local descriptor table descriptor.

49. The computer readable medium as recited in claim 34 wherein said first storage location is a memory location.

50. The computer readable medium as recited in claim 34 wherein said first storage location is a general purpose register within said processor.

51. The computer readable medium as recited in claim 34 wherein said first storage location is a special purpose register within said processor.

X. EVIDENCE APPENDIX

No evidence submitted under 37 CFR §§ 1.130, 1.131 or 1.132 or otherwise entered by the Examiner is relied upon in this appeal.

XI. RELATED PROCEEDINGS APPENDIX

There is no decision received by Appellant in the related proceeding.